

# Preface

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This is a book for semiconductor design engineers working on analog and mixed-signal integrated circuits; however, it also contains useful information for package, printed circuit board, and system designers. The book provides a practical approach to the analysis of noise coupling mechanisms, the implementation of suppression techniques, and the simulation using modeling and extraction tools. The overall goal is to improve the technical skills of designers, enabling them to better understand and solve the continuously aggravating noise coupling issues.

The first two chapters discuss fundamental concepts governing noise coupling mechanisms and present an overview of integrated circuits fabrication technology. The purpose is to prepare readers for the material presented in the following chapters.

Chapters three, four, and five focus on understanding the physical mechanisms that govern the noise coupling in integrated circuits. Noise generation, propagation and reception are analyzed at the device structure, chip, package and printed circuit board levels. Emphasis is placed on building or improving analysis skills of the noise coupling phenomenon, so that readers can apply the knowledge and techniques learned here to existing and future devices and technologies.

Chapter six focuses on measuring the noise coupling in integrated circuits. It emphasizes that the measurement process should not interfere with circuits by either changing the noise propagation or inserting additional noise from its own circuits. Various techniques are presented, and advantages and disadvantages are discussed. A novel technique using differential sensors for power and substrate noise and an on-chip waveform digitizer is presented. Readers learn how to perform accurate measurements and how to avoid the contamination of results from crosstalk or ground bounce.

Chapter seven focuses on suppressing the noise coupling in integrated circuits. Advantages, disadvantages, and limitations of various techniques are presented with relation to the physical structures of devices and substrate. Emphasis is placed on suppression by properly designing the power distribution at the system, board, package, and chip levels. The analysis results suggest that the choice and efficiency of suppression techniques

depend directly on the specific noise coupling mechanisms of each individual case. To overcome the limitations of traditional suppression techniques, additional circuit level compensation may be considered. This chapter presents two design examples of circuit level compensation techniques and the experimental results from test chip measurements. The detailed presentations of these two techniques show the development procedures and the experimental results. These development procedures can serve as models for the design of noise cancellation techniques in other applications.

Chapter eight focuses on modeling and simulating the noise coupling in integrated circuits. The selection choice and use of conventional methods and tools are discussed, highlighting the advantages and limitations specific to various stages of the design flow. The importance of being able to predict the noise coupling early in the architectural stages of the design is emphasized. Since most of the existing tools do not offer a practical approach to noise coupling simulation in early stages, this chapter presents a modeling technique based only on the information typically available in the architectural definition stages of projects. The model is constructed based on the physical structure of devices, technology parameters available in the design guide, and statistical data from typical practices or previous designs. An example showing the model construction and correlation with measurements on a test chip is presented.

## A Note to the Reader

Reading this book may raise technical questions or generate discussions. Please send us your comments and feedback either through the “Contact Us” form available on the web site <http://www.noisecoupling.com>, or by mail to:

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