Figures 5.9 (b) shows a model of the noise reception in an emitter-follower NPN transistor. Notice that, because of the low impedance of the *VCC2* supply, the substrate noise coupling into the emitter-follower NPN is negligible. However, the noise on the *VCC2* supply may couple into the substrate trough the junction capacitance of the buried layer, C_{NBL}.

The noise reception mechanism in common-base NPN is similar to the noise reception in common-emitter NPN, as modeled in Figure 5.9 (c). The difference between the *VCC2* and *VEE2* waveforms is seen as power supply noise. The substrate noise couples into the collector through the junction capacitance of the buried layer, C_{NBL}. The substrate noise coupled into the base and emitter is negligible.

5.3.2 Noise Reception in PNP Transistors

Figure 5.10 illustrates the noise reception mechanisms in a lateral PNP transistor. This transistor is shown in common-emitter configuration; however, other configurations can be analyzed in a similar way. The noise generator circuits on the chip are symbolically represented by the *aggressor* circuit. The power supplies of the PNP transistor, *VCC2* and *VEE2*, are provided separately from the power supplies of the *aggressor* circuit. PNP transistors in circuits powered from the same supplies as the *aggressor* can be analyzed similarly, by replacing the noise waveforms on *VCC2* and *VEE2* nodes with the waveforms on *VCC1* and *VEE1* nodes, respectively.

The *aggressor* circuit generates noise on the *VCC1* and *VEE1* supplies and in the substrate, as shown by the positive and negative voltage spikes in the figure. These voltage spikes propagate through the power distribution and the common substrate to other regions of the chip.

The noise waveforms coupled into the *VCC2* and *VEE2* supplies depend on the power distribution architecture on the chip, package, and PCB. The power supply noise waveforms shown in this figure correspond to the mechanism of coupling through shared impedance. These waveforms may change for other coupling mechanisms of the power distribution circuit.

The difference between the *VCC2* and *VEE2* waveforms is seen as power supply noise by the common-emitter PNP circuit. The substrate noise couples into the base of the transistor through the junction capacitance of the buried layer. The magnitude of the coupled noise depends on the junction capacitance and circuit impedance at the base node. Higher impedance nodes

couple larger magnitude of noise compared to lower impedance nodes.

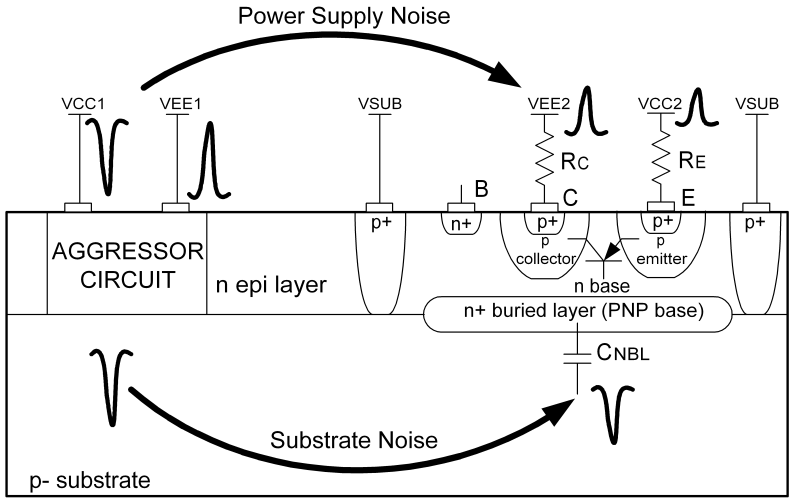

Figure 5.10 Noise reception mechanisms in a common-emitter PNP transistor.

The junction capacitance increases with the transistor size. The value of this capacitance can be calculated from the design manual specifications or can be obtained using layout extraction tools. The base node impedance can be calculated from the circuit topology and the component values. The substrate noise coupled into the collector and emitter is negligible.

Figure 5.11 (a) shows a circuit level model of this coupling mechanism. The voltage spikes represent the noise waveforms on the substrate and power supplies.

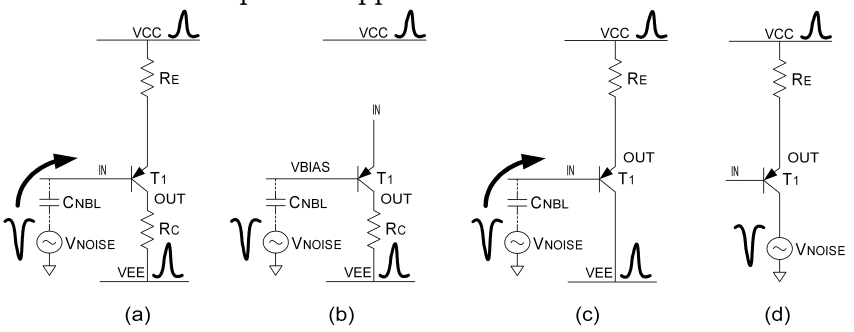

Figure 5.11 Models of the noise reception by common-emitter (a), common-base (b), emitter-follower (c), lateral PNP transistors, and emitter-follower (d) substrate PNP transistors.

The difference between the power supply waveforms is seen as power supply noise by circuits. The substrate noise, represented by V_{NOISE}, is injected into the base through the junction capacitance of the buried layer, C_{NBL}.

Figure 5.11 (b) shows the noise reception model for the common-base configuration. Since the *VBIAS* supply has typically low impedance, the substrate noise coupling into the base is negligible.

Figure 5.11 (c) shows the noise reception model for the emitter-follower configuration. The difference between the *VCC2* and *VEE2* waveforms is seen as power supply noise. The substrate noise couples into the base through the junction capacitance of the buried layer, C_{NBL}.

Figure 5.11 (d) shows the noise reception mechanism by the substrate PNP in emitter-follower configuration. Since the collector is electrically connected to the substrate, the substrate noise shows directly on the collector. The coupling into the emitter and base is negligible.

SUMMARY

- NPN transistors receive substrate noise only through collectors. The magnitude of the coupled noise depends on device size and circuit impedance at the collector node.
- The substrate noise received by emitter-follower NPN transistors is negligible.
- Lateral PNP transistors receive substrate noise only through bases. The magnitude of coupled noise depends on device size and circuit impedance at the base node.
- The substrate noise received by common-base PNP transistors is negligible.
- Substrate PNP transistors receive substrate noise directly on the collector terminal.

5.4 NOISE RECEPTION IN MOS TRANSISTORS

5.4.1 Noise Reception in NMOS Transistors

Figure 5.12 illustrates the noise reception mechanisms in an NMOS transistor. This transistor is shown in common-source configuration; however, other configurations can be analyzed in a similar way.

In mixed-signal CMOS integrated circuits the majority of noise is generated by the digital switching circuits and couples into the sensitive analog circuits. In Figure 5.12 the noise generator circuits are represented by the *aggressor* and the sensitive circuits by the NMOS transistor. Separate power supplies are applied to the NMOS transistor, represented by *VDDA* and *VSSA*, and to the *aggressor* circuit, represented by *VDDD* and *VSSD*.

NMOS transistors in circuits powered from the same supply as the *aggressor* can be analyzed similarly by replacing the noise waveforms on *VDDA* and *VSSA* nodes with the waveforms on *VDDD* and *VSSD* nodes, respectively.

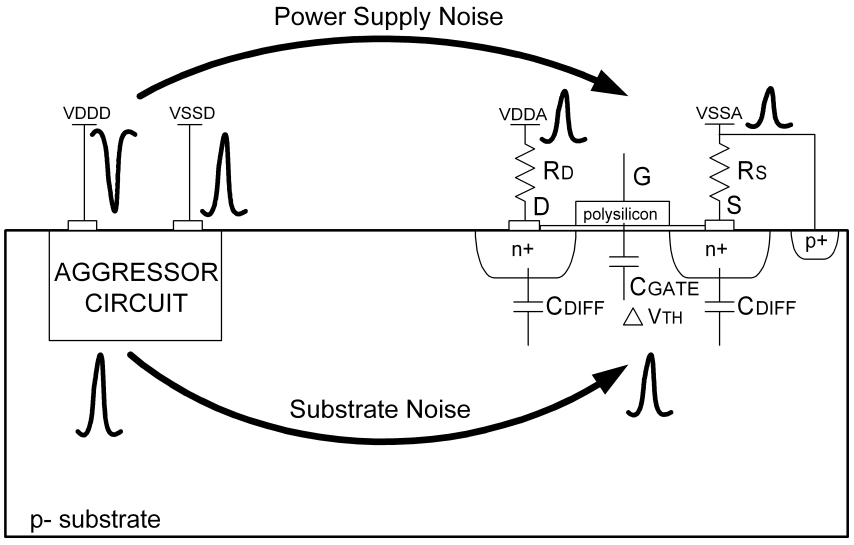

Figure 5.12 Noise reception mechanisms in a common-source NMOS transistor.

The *aggressor* circuit generates noise on the *VDDD* and *VSSD* supplies and in the substrate, as shown by the positive and

negative voltage spikes in the figure. These voltage spikes propagate through the power distribution and the common substrate to other regions of the chip.

The noise waveforms coupled into the *VDDA* and *VSSA* supplies depend on the power distribution architecture on the chip, package, and PCB. The positive voltage spikes shown in this figure correspond to the noise propagation example discussed in Chapter 4, which used a common *VSS* node in the package. Other power distribution architectures may result in different noise waveforms. The difference between the *VDDA* and *VSSA* waveforms is seen as power supply noise by the common-source NMOS circuit.

The substrate noise interacts with the NMOS transistor primarily through the source and drain junction capacitances and through the body-effect. These two mechanisms are illustrated by C_{DIFF} and ΔV_{TH} in the figure. The capacitance of the reversed biased junctions acts as a direct coupling path between the substrate and the drain, and between the substrate and the source. The body-effect is manifested as threshold voltage modulation by the substrate noise. To illustrate this effect, let's look at the square-law *I-V* characteristic of an NMOS transistor:

$$I_D = \frac{1}{2}\mu \cdot C_{OX} \cdot \left(\frac{W}{L}\right) \cdot \left(V_{GS} - V_T\right)^2 \tag{5.1}$$

where

I_D = drain current
μ = mobility
C_{OX} = gate oxide capacitance
V_{GS} = gate to source voltage
V_T = threshold voltage.

The threshold voltage depends on the potential difference between source and substrate, V_{SB}, following the relation

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{\left|2 \cdot \phi_F\right| + V_{SB}} - \sqrt{\left|2 \cdot \phi_F\right|}\right) \tag{5.2}$$

where

V_{T0} = the threshold voltage with $V_{SB} = 0$
γ = the body effect parameter
$2\Phi_F$ = the surface potential parameter

The substrate noise is reflected in V_{SB} voltage variations, which further affect V_T and I_D. The variation of the drain current,

I_D, induced by the substrate noise affects the performance of circuits.

Figure 5.13 shows a model of the noise reception in a common-source NMOS transistor.

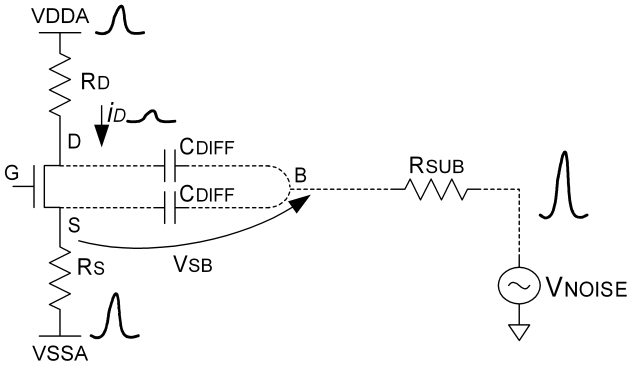

Figure 5.13 Model of the noise reception in a common-source NMOS transistor.

The difference between the *VDDA* and *VSSA* waveforms is seen as power supply noise. The source and drain diffusion capacitance, C_{DIFF}, provides *AC* coupling paths with the substrate. The substrate noise couples through threshold modulation into the drain current, as shown by the i_D current pulse waveform in the figure.

5.4.2 Noise Reception in PMOS Transistors

Figure 5.14 illustrates the noise reception mechanisms in a PMOS transistor in common-source configuration. The noise generator circuits on chip are symbolically represented by the *aggressor* circuit. Separate power supplies are applied to the PMOS transistor, represented by *VDDA* and *VSSA*, and to the *aggressor* circuit, represented by *VDDD* and *VSSD*.

PMOS transistors in circuits powered from the same supplies as the *aggressor* can be analyzed similarly by replacing the noise waveforms on *VDDA* and *VSSA* nodes with the waveforms on *VDDD* and *VSSD* nodes, respectively.

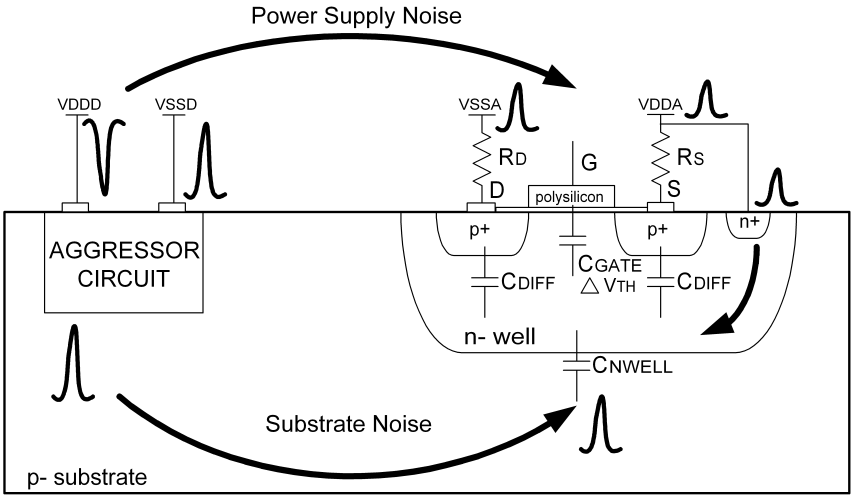

Figure 5.14 Noise reception mechanisms in a common-source PMOS transistor.

The *aggressor* circuit generates noise on the *VDDD* and *VSSD* supplies and in the substrate, as shown by the positive and negative voltage spikes in the figure. These voltage spikes propagate through the power distribution and the common substrate to other regions of the chip.

Similarly to the NMOS analysis, the power supply noise waveforms shown in the figure correspond to the mechanism of coupling through shared impedance, discussed in Chapter 4. These waveforms may change for other coupling mechanisms of the power distribution circuit. The difference between the *VDDA* and *VSSA* waveforms is seen as power supply noise by the common-source PMOS circuit.

The bulk node of the PMOS transistor is electrically connected to the n-well. This n-well receives noise from the *VDDA* supply through the biasing contacts and from the underlying substrate through the interface junction capacitance. In circuits closer to the *aggressor*, the substrate noise dominates, and in circuits located far from the *aggressor*, the *VDDA* noise dominates.

The n-well noise interacts with the PMOS transistor through the source and drain junction capacitance and through the body-effect. These two mechanisms are illustrated by C_{DIFF} and ΔV_{TH} in the figure. The capacitance of the reversed biased junctions acts